From studying NPN transistors and the bipolar logic circuits that they form, it becomes apparent why the common terms V_{CC} and V_{EE} have come to represent the positive and negative supply voltages in a digital circuit. Bipolar logic has the collectors of its NPN transistors connected to the positive supply voltage and its emitters connected to the negative supply voltage—usually ground, but not always.

13.7 FIELD-EFFECT TRANSISTORS

Metal oxide semiconductor (MOS) technology represents the vast majority of transistors used to implement digital logic on integrated circuits ranging from logic devices to microprocessors to memory. Most *field-effect transistors* (FETs) are fabricated using MOS technology and are called MOSFETs. (The JFET is an exception to this and is briefly mentioned at the end of this chapter. This discussion uses the term *FET* in reference to a MOSFET.) Figure 13.19 shows the general structure of an *enhancement-type* FET. Just as BJTs are available in NPN and PNP according to the doping of their regions, there are n-FETs and p-FETs, referred to as NMOS and PMOS technologies, respectively. A FET consists of two main conduction regions, one called the *source* and the other the *drain*. In an n-FET, the source and drain are both N-type silicon. A channel of oppositely doped silicon separates the source and drain. Without any external influence, there is no conduction across the channel, because one pn junction is always reverse biased. A third terminal, the *gate*, is the control element that enables conduction across the channel. The gate is insulated from the rest of the FET by a thin layer of silicon dioxide (SiO_2). As the gate voltage is increased relative to the source voltage in an n-FET, the electric field developed at the gate causes a portion of the channel to change its electrical properties. The channel begins to behave as if it were doped the same way as the source and drain, enabling current to flow between the source and drain.

Whereas a BJT's conduction between emitter and collector is a function of its base current, a FET's conduction is a function of the gate-source voltage, V_{GS}, and the drain-source voltage, V_{DS}. An n-FET begins to conduct when V_{GS} exceeds the *threshold voltage*, V_T. In a typical circuit configuration, the drain is at a higher voltage than the source and current flows from drain to source. Current flowing into the drain, I_D, equals current flowing out of the source, I_S, because current cannot flow into or out of the insulated gate ($I_G = 0$). For a fixed $V_{GS} > V_T$, the relationship between I_D and V_{DS} is a curve that starts out nearly linear and then begins to taper off as V_{DS} increases, as shown in Fig. 13.20. The region in which I_D increases with V_{DS} is called the *triode region*. For small V_{DS}, the V_{GS}-induced channel presents very little resistance, and I_D increases almost in a linear manner with respect to V_{DS}. As V_{DS} and I_D increase, the resistance of the induced channel begins to increase, causing the curve's slope to decrease. At a certain point, the FET saturates and can conduct no more current even as V_{DS} continues to increase. The saturation voltage, $V_{DS\,(SAT)}$, equals $V_{GS} - V_T$. Increasing V_{GS} increases the saturation point, enabling more current to flow through the transistor.

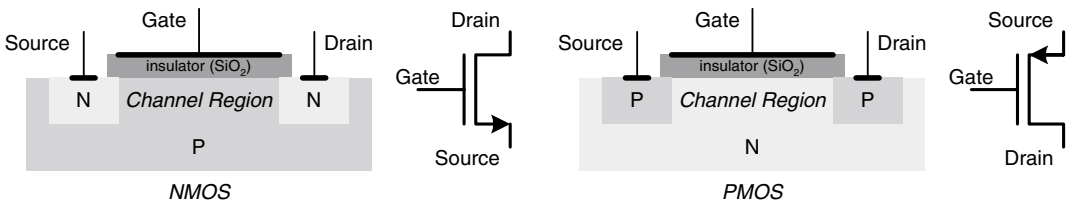

FIGURE 13.19 NMOS and PMOS enhancement-type FET structures and graphical representations.

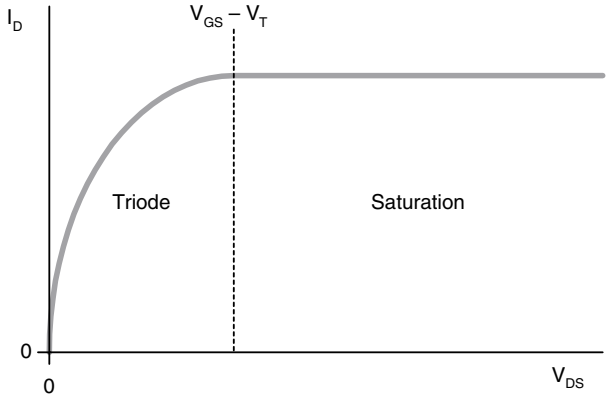

FIGURE 13.20 Enhancement-type n-FET I_D vs. V_{DS} for fixed $V_{GS} > V_T$.

The I_D/V_{DS} curve can be mathematically calculated, but the formulas require knowledge of specific physical parameters of a transistor's fabrication process. When integrated circuits are designed, such information is critical to device operation, and manufacturing process parameters are at an engineer's disposal. Data sheets for discrete FETs, however, do not typically provide the detailed process parameters required for these calculations. Instead, manufacturers provide device characterization curves in their data sheets that show I_D/V_{DS} curves for varying V_{GS}. An example of this is the graph contained in Fairchild Semiconductor's 2N7002 NMOS transistor data sheet and shown in Fig. 13.21. PMOS transistors function in the same manner as NMOS, although the polarities are reversed. The source is typically at a higher voltage than the drain, and V_{GS} is expressed as a negative value.

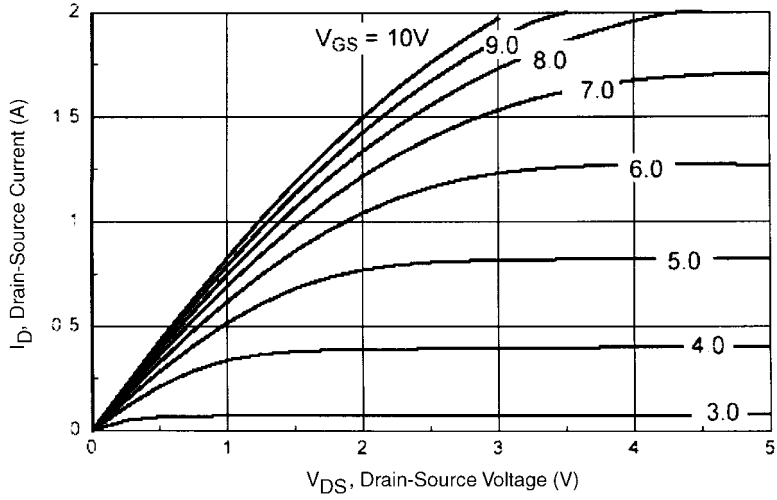

FIGURE 13.21 2N7002 I_D/V_{DS} graph. *(Reprinted with permission from Fairchild Semiconductor and National Semiconductor.)*